REMARKS/ARGUMENTS

Brief Summary of Status

Claims 30-58 are pending in the application.

Claims 35-58 are allowed.

Claims 30, 32-34 are rejected.

Claims 31 objected to.

Requested Clarification from Examiner

a. In the "Office Action Summary" (PTOL-326 (Rev. 1-04), which is page 2 of the office action, the Examiner indicates that claims 30, 32-34, and 43-58 are rejected.

However, the Examiner indicates that claims 35-58 are allowed on p. 3 of the office action.

"***Allowable Subject Matter***

Claims 35-58 are allowed." (office action, Part of Paper No./Mail Date 10, p. 3)

The Applicant assumes that the Examiner inadvertently made a typographical error on the "Office Action Summary" (PTOL-326 (Rev. 1-04), which is page 2 of the office action.

As such, the Applicant assumes that the Examiner has allowed claims 35-58, as indicated on page 3 of the office action.

b. In the "Office Action Summary" (PTOL-326 (Rev. 1-04), which is page 2 of the office action, the Examiner indicates that the action is non-final, and this is how the Applicant docketed this office action during its preliminary processing.

However, the Examiner indicates on p. 3-4 of the office action that "THIS ACTION IS MADE FINAL"

The Examiner asserts:

"**THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the

shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action." (office action, Part of Paper No./Mail Date 10, p. 3-4)

Given that the check box as indicated on the "Office Action Summary" (PTOL-326 (Rev. 1-04), which is page 2 of the office action, indicated that the action was non-final, the Applicant assumes that the Examiner means for this action to be non-final.

In an effort to ensure that the Examiner gets the response to the office action expeditiously in any event, the Applicant mails this response to "Mail Stop AF".

c. Moreover, given the various inconsistencies between the "Office Action Summary" (PTOL-326 (Rev. 1-04), which is page 2 of the office action and the actual text of the office action (i.e., at least with respect to allowed vs. non-allowed claims, whether or not the office action is "final" or "non-final", and the previously non-entered amendment with respect to the "attorney docket number"), the Applicant respectfully requests that the Examiner lean towards the option of these various inconsistencies in a manner that is the least detrimental to the Applicant. For example, the Applicant respectfully requests that the Examiner honor the Applicant's good-faith reliance on the allowability of claims 35-58 as well as the Applicant's good-faith reliance that this office action is in fact non-final.

If any of the assumptions made by the Applicant are incorrect, the Applicant respectfully requests immediate clarification from the Examiner.

Double Patenting (Provisional Rejection under 35 U.S.C. § 101)

1. The Examiner asserts:

"Claim 34 is provisionally rejected under 35 U.S.C. 101 as claiming the same invention as that of claim 30 of this application. This is a provisional double patenting rejection since the conflicting claims have not in fact been patented." (office action, Part of Paper No./Mail Date 10, p. 2)

The Applicant respectfully traverses.

The Applicant has amended certain of the claims.

The Applicant respectfully points out that claim 34 includes limitations that claim 31 does not. Claim 34 includes the limitations that "the positive end of the first output impedance is coupled to a voltage supply" and that "the positive end of the second output impedance is coupled to the voltage supply". Claim 31 does not include these limitations, as such, each of the first output impedance and the second output impedance of claim 31 need not be connected to the voltage supply, or could alternatively be connected to different voltage supplies, or could alternatively be connected to yet another impedance, among other possible connections. The connectivity of each of the "positive end of the first output impedance" and the "positive end of the second output impedance" is not limited within claim 31.

As such, claim 34 claims subject matter that is distinct and different from claim 31. Therefore, the Applicant respectfully requests that the Examiner withdraw the provisional rejection of claim 34 under 35 U.S.C. § 101.

35 U.S.C. §103(a)

2. The Examiner asserts:

"Claims 30-34 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wakimoto et al., U.S. patent # 4,885,548." (hereinafter referred to as "Wakimoto") (office action, Part of Paper No./Mail Date 10, p. 2)

The Examiner also asserts:

"Fig. 4 of Wakimoto et al. discloses a circuit comprising: transistors 5 and 6 can be read as a first and a second differential transistors; current source 9 can be read as a current source; capacitors 13 and 14 can be read as a first and a second miller capacitance cancellation capacitors; resistors 7 and 8 can be read as a first and a second output impedances.

Although Wakimoto et al. uses bipolar transistors instead of field effect transistors as claimed, they are just different types of transistors; therefore, it would have been obvious at the time the invention was made to a person having ordinary skill in the art to

substitute field effect transistors for bipolar transistors in the circuit of Wakimoto et al. in the absence of unexpected results since such substitution is well known in the art.

Regarding claims 32 and 33, although Wakimoto et al. only shows a current source instead of a transistor or a NMOS, PMOS transistor, Momtaz et al. teaches in Fig. 2 the use of a CMOS transistor for the current source; thus, it would have been obvious at the time the invention was made to a person having ordinary skill in the art to use the teaching of Momtaz et al. in the circuit of Wakimoto et al. since this is a well known practice in the art." (office action, Part of Paper No./Mail Date 10, p. 2-3)

The Applicant respectfully traverses.

The Applicant has amended certain of the claims.

The Applicant respectfully asserts that Wakimoto fails to teach and disclose the subject matter of claim 30 that includes at least an amplifier stage, comprising: a current source; a first differential transistor having a source, gate, and drain, wherein the source of the first differential transistor is coupled to the current source; a second differential transistor having a source, gate, and drain, wherein the source of the second differential transistor is coupled to the current source; a first output impedance having positive and negative ends, wherein the negative end of the first output impedance is coupled to the drain of the first differential transistor and wherein the first output impedance includes a first shunt peaking inductor; a second output impedance having positive and negative ends, wherein the negative end of the second output impedance is coupled to the drain of the second differential transistor and wherein the second output impedance includes a second shunt peaking inductor; a first miller capacitance cancellation capacitor having positive and negative ends, wherein the positive end of the first miller capacitance cancellation capacitor is coupled to the drain of the second differential transistor, and wherein the negative end of the first miller capacitance cancellation capacitor is coupled to the gate of the first differential transistor; and a second miller capacitance cancellation capacitor having positive and negative ends, wherein the positive end of the second miller capacitance cancellation capacitor is coupled to the drain of the first differential transistor, and wherein the negative end of the second miller capacitance cancellation capacitor is coupled to the gate of the second differential transistor.

As such, the Applicant respectfully believes that claim 30 is patentable over Wakimoto.

In addition, the Applicant respectfully believes that claims 31-34, being further limitations of the subject matter as claimed in claim 30, are also allowable.

Allowable Subject Matter

Claims 35-58 are allowed.

The Applicant respectfully believes that claims 30-58 are in condition for allowance and respectfully requests that they be passed to allowance.

The Examiner is invited to contact the undersigned by telephone or facsimile if the Examiner believes that such a communication would advance the prosecution of the present U.S. utility patent application.

RESPECTFULLY SUBMITTED,

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